IN THE CLAIMS

We claim:

1. A transistor comprising:

a channel region formed from a narrow bandgap semiconductor film formed on insulating substrate;

a gate dielectric formed on said low bandgap semiconductor film;

a gate electrode formed on said gate dielectric; and

a pair of source/drain regions formed from a semiconductor film having a wider bandgap than said low bandgap semiconductor film formed on opposite sides of said gate electrode and adjacent to said low bandgap semiconductor film.

2. The transistor of claim 1 wherein said narrow bandgap semiconductor film has a bandgap of less than or equal to 0.7 eV.

3. The transistor of claim 1 wherein said narrow bandgap semiconductor film comprises InSb.

4. The transistor of claim 2 wherein said low bandgap semiconductor film is selected from the group consisting of InAs, PdTe and InSb.

5. The transistor of claim 1 wherein said gate dielectric comprises a high dielectric constant film.

6. The transistor of claim 1 wherein said source and drain regions are formed from a III-V semiconductor.

7. The transistor of claim 1 wherein said gate electrode is a metal gate electrode.

8. The transistor of claim 1 wherein the bandgap of said semiconductor film of said source/drain regions is at least 0.2 eV greater than the bandgap of said channel region.

9. The transistor of claim 1 wherein said semiconductor film of said source/drain regions is selected from the group consisting of InAlSb, InP, GaSb, GaP, and GaAs.

10. A transistor comprising:

a channel region formed from narrow bandgap semiconductor film formed on an insulating substrate;

a gate dielectric formed on said narrow bandgap semiconductor film;

a gate electrode formed on said gate dielectric; and

a pair of metal source/drain regions formed along opposite sides of said gate electrode and adjacent to said narrow bandgap semiconductor film.

11. The transistor of claim 10 wherein said low bandgap semiconductor film has a bandgap of less than or equal to 0.7 eV.

12. The transistor of claim 10 wherein said low bandgap semiconductor film is selected from the group consisting of InAs, PdTe and InSb.

13. The transistor of claim 10 wherein said source/drain regions are formed from a material selected from the group consisting of titanium nitride, tantalum nitride and hefium nitride.

14. The transistor of claim 10 wherein said source/drain regions are formed from a metal film which can form a Schottky barrier with said low bandgap semiconductor film.

15. The transistor of claim 10 wherein said metal film is selected from the group consisting of platinum, aluminum and gold.

16. The transistor of claim 10 wherein said gate dielectric has a dielectric constant greater than 9.0.

17. The transistor of claim 10 wherein said gate dielectric comprises a metal oxide dielectric.

18. The transistor of claim 10 wherein said gate dielectric layer is selected from the group consisting of PZT, BST, tantalum pentaoxide, hefium oxide, zirconium oxide and aluminum oxide.

19. The transistor of claim 10 wherein said gate dielectric layer has a thickness between 20-3000Å.

20. The transistor of claim 10 wherein said gate electrode comprises a metal film.

21. The transistor of claim 10 wherein said gate electrode has a midgap work function.

22. The transistor of claim 10 wherein said transistor has a gate length of less than or equal to 30 nanometers.

23. The transistor of claim 10 wherein said thickness of said low bandgap semiconductor film is approximately 1/3 the gate length of said transistor.

24. The transistor of claim 10 wherein said insulating substrate comprises a silicon dioxide film formed on a monocyrstalline silicon substrate.

25. A transistor comprising:

an InSb alloy film formed on an oxide film formed on a monocrystalline silicon substrate;

a gate dielectric layer formed on said InSb alloy film wherein said gate dielectric is a high dielectric constant film;

a metal gate electrode formed on said gate dielectric layer; and

a source region and a drain regions formed on opposite sides of said gate electrode adjacent to said InSb alloy film and on said oxide film, said source and drain regions formed from a metal film.

26. The transistor of claim 25 wherein said metal film is selected from a material which can form a Schottky barrier with said InSb alloy.

27. The transistor of claim 25 wherein said metal film is selected from the group consisting of titanium nitride, tantalum nitride and hefium nitride.

28. A transistor comprising:

an InSb alloy film formed on an oxide film formed on a monocrystalline silicon substrate;

a gate dielectric layer formed on said InSb alloy film wherein said gate dielectric is a high dielectric constant film;

a metal gate electrode formed on said gate dielectric layer; and

a source region and a drain regions formed on opposite sides of said gate electrode adjacent to said InSb alloy film and on said oxide film, said source and drain regions formed from a semiconductor film having a wide bandgap.

29. The transistor of claim 28 wherein said semiconductor film is selected from the group consisting of InP, GaSb, GaP, and GaAs.

30. The transistor of claim 28 wherein said gate dielectric is selected from the group consisting of PZT, BST, tantalum pentaoxide, hefium oxide, zirconium oxide and aluminum oxide.

31. A method of forming a transistor comprising:

forming a narrow bandgap semiconductor film on an insulating substrate;

forming a gate dielectric layer on said narrow bandgap semiconductor film;

forming a gate electrode on said gate dielectric; and

forming a pair of source/drain regions adjacent to said narrow bandgap semiconductor film.

32. The method of claim 31 wherein said narrow bandgap semiconductor film has a bandgap of less than or equal to 0.7 eV.

33. The method of claim 32 wherein said narrow bandgap semiconductor film is selected group consisting of InAs, PdTe and InSb.

34. The method of claim 32 wherein said source/drain regions are formed from a semiconductor film having a larger bandgap then said narrow bandgap semicomductor film.

35. The method of claim 31 wherein said source/drain regions are formed from a compound semiconductor.

36. The method of claims 34 wherein said semiconductor film of said source/drain regions is selected from the group consisting of InAlSb, InP,GaSb, GaP, and GaAs.

37. The method of claim 31 wherein said source/drain regions are formed from a metal film.

38. The method of claim 37 wherein said metal film forms a Schottky barrier with said narrow bandgap semiconductor film.

39. The method of claim 37 wherein said metal film is selected from the group consisting of titanium nitride, tantalum nitride and hefium nitride.

40. The method of clam 31 wherein said gate dielectric layer comprises a deposited high dielectric constant film.

41. The method of claim 31 wherein said gate electrode comprises a metal film.

42. A method of forming a transistor comprising:

forming an InSb alloy film on an insulating substrate;

forming a high dielectric constant gate dielectric film on said InSb alloy film;

forming a metal gate electrode on said gate dielectric layer; and

forming a pair of source/drain regions on opposite sides of said gate electrode on said insulating substrate.

43. The method of claim 42 wherein said source/drain regions are formed from a metal film.

44. The method of claim 42 wherein said source/drain regions are formed from a wide bandgap semiconductor film.

45. A transistor comprising:

a channel region formed from a narrow bandgap semiconductor film formed on insulating substrate;

a gate dielectric formed on said narrow bandgap semiconductor film;

a gate electrode formed on said gate dielectric; and

a pair of source/drain regions formed on said insulating substrate and adjacent to opposite sides of said narrow bandgap semiconductor film.

46. The transistor of claim 45 wherein said source/drain regions are formed from a metal film.

47. The transistor of claim 45 wherein said source/drain regions are formed from a wide bandgap semiconductor film.